[METHOD OF FABRICATING A MOS TRANSISTOR WITH A SHALLOW JUNCTION]

Abstract of Disclosure

A semiconductor wafer is provided having both a memory array area and a periphery circuit region defined on the surface of the semiconductor wafer. A gate composed of a silicon oxide layer and a silicon germanium layer is formed on the surface of the periphery circuit region, and a spacer, a source and a drain of the MOS transistor are formed around the gate. Finally, a nickel (Ni) layer is formed on the surface of the source and the drain, and a rapid thermal annealing process (RTA process) with a temperature ranging between 400 ° Cand 500 ° C is performed for forming a silicon nickel layer on the surface of the source and the drain. Additionally, a shallow junction for the source and the drain is formed.

Figures